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[METHOD OF FABRICATING THIN FILM TRANSISTOR ARRAY SUBSTRATE AND STACKED THIN FILM STRUCTURE]

Abstract

A method of fabricating a thin film transistor array substrate is provided. First, a first patterned metallic layer, a dielectric layer, an amorphous silicon layer, a second patterned metallic layer and a passivation layer are sequentially formed over a substrate. A patterned photoresist layer is formed over the passivation layer. The patterned photoresist layer at least covers the source/drain (formed out of the first patterned metallic layer) as well as the area beside them. The edges of the patterned photoresist layer have a plurality of thin-out regions. Each thin-out region stretches across part of the edge of one source/drain. Thereafter, using the patterned photoresist layer as an etching mask, an etching operation is carried out until the source/drain and its peripheral amorphous silicon layer under the thin-out regions are exposed to form a plurality of staircase structures. Finally, a plurality of pixel electrodes is formed over the substrate to cover the respective staircase structures and electrically connect to one

source/drain electrode.